“Near Ideal” 30-V N-Channel MOSFET Technology

This document provides a summary of preliminary performance on SkyWater Technology’s proprietary new MOSFET technology. Additional Min/Max information and parametric plots will be provided in subsequent updates. The underlying process technology is currently in qualification and is expected to be released to production near the end of the second quarter of 2022. A limited quantity of coupon boards and packaged samples available now, with higher quantities coming in 2Q2022.

Summary:

A novel device architecture enables a new level of low-voltage MOSFET performance. The technology enables 2x lower output charge (Q_{oss}) and superior specific on-resistance ($SR_{DS(ON)}$) compared to current <60V MOSFETs. Near-zero reverse-recovery charge/losses enable high-speed switching, low leakage, improved efficiency, and potential removal of external Schottky diodes. Initially offered as a 30V device, this foundry technology will be open for custom design for different power levels through a factory-supported PDK.

Features:

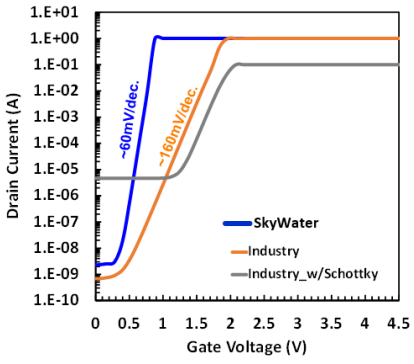
- Ultra-low output charge and Drain-Source capacitance
- Ultra-low $R_{DS(ON)}$
- Low 2.5-V logic-level gate drive

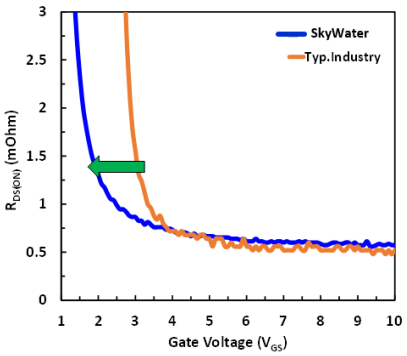
Benefits:

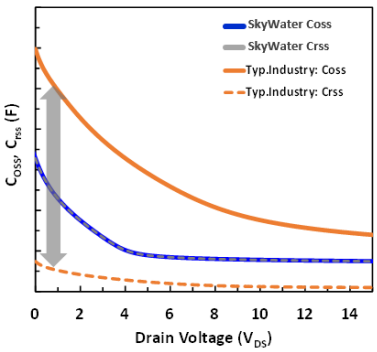
- Elimination of Drain-Source coupling enables near-zero reverse recovery losses
- Improved design- and system-level efficiency
- Simplifies system design

Sample Applications:

- DC/DC Conversion
- ORing and Load Switch
- Battery Management
- Motor Control
- Active Rectification
- System-in-Package (SiP) Designs







STATIC CHARACTERISTICS (T_J=25°C unless otherwise noted)						
Symbol	**Parameter**	**Conditions**	**Min**	**Typ**	**Max**	**Units**
BV_{DSS}	Drain-Source Breakdown Voltage	I_D=250uA,V_{GS}=0V	30			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=30V,V_{GS}=0V		5nA	1	µA
		T_J=55°C			5	
I_{GSS}	Gate-Body leakage current	V_{DS}=0V,V_{GS}=+/-12V			100	nA
$V_{GS(th)}$	Gate Threhold Voltage	V_{DS}=V_{GS},I_D=250uA		0.7		V
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS}=4.5V,I_D=20A		2.01		mΩ
		T_J=125°C				
		V_{GS}=3.3V,I_D=20A		2.2		mΩ
		V_{GS}=2.5V,I_D=20A		2.4		mΩ
DYNAMIC CHARACTERISTICS (T_J=25°C unless otherwise noted)						
Symbol	**Parameter**	**Conditions**	**Min**	**Typ**	**Max**	**Units**
C_{iss}	Input Capacitance (Cgs+Cgd)	V_{GS}=0V,V_{DS}=12V,f=1MHz		2487		pF
C_{oss}	Output Capacitance (Cds+Cgd)			290		pF
C_{rss}	Reverse Transfer Capacitance (Cgd)			289		pF
R_g	Gate Resistance	f=1MHz				Ω
$t_{d(on)}$	Turn-on delay time	V_{GS}=4.5V, V_{DS}=12V, R_G=1.6Ω, I_D=20A		0.22		ns
t_r	Rise time			1.93		ns
$t_{d(off)}$	Turn-off delay time			23.47		ns
t_f	Fall time			14.42		ns

GATE CHARGE CHARACTERISTICS (T_J=25°C unless otherwise noted)						
Symbol	**Parameter**	**Conditions**	**Min**	**Typ**	**Max**	**Units**
Q_g(4.5V)	Total Gate Charge	V_{GS}=4.4V/3.3V/2.5V,V_{DS}=12V,I_D=20A		35.2		nC
Q_g(3.3V)	Total Gate Charge			26.6		nC
Q_g(2.5V)	Total Gate Charge			20.6		
Q_{gs}	Gate Source Charge			1.47		nC
Q_{gd}	Gate Drain Charge			6.13		nC
Q_{OSS}	Output Charge	V_{DS}=12V		4.7		nC
SOURCE-DRAIN CHARACTERISTICS (T_J=25°C unless otherwise noted)						
Symbol	**Parameter**	**Conditions**	**Min**	**Typ**	**Max**	**Units**
V_{SD}	Diode Forward Voltage	I_S=1A,V_{GS}=0V		0.72		V
Q_{IT}	Body Diode Reverse Recovery Charge	I_F=20A,di/dt=500A/us		~0		nC

Maximum Ratings for QFN & Similar Package				
Symbol	**Parameter**	**Conditions**	**Maximum**	**Units**
V_{DS}	Drain-Source Voltage	-	30	V
V_{GS}	Gate-Source Voltage	-	±10	V
I_D	Continuous Drain Current	T_C=25°C	160	A
		T_C=100°C	125	A
I_{DM}	Pulsed Drain Curretn	<10us	700	A

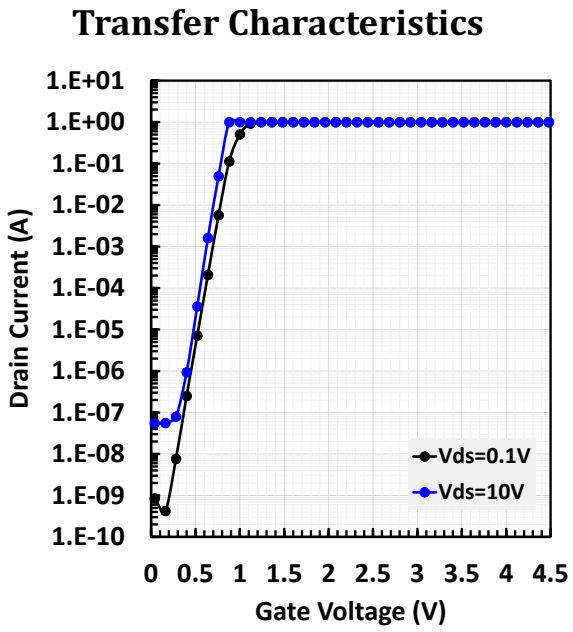


Figure 1: Typical measured transfer characteristics. On current limited by compliance limit.

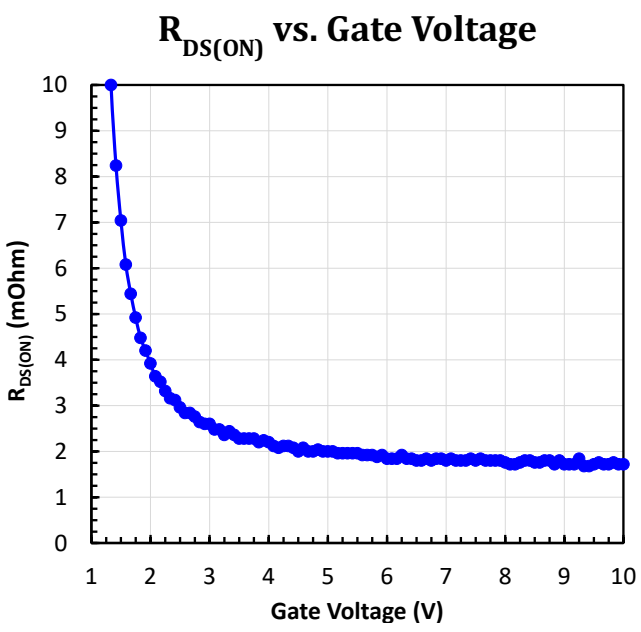


Figure 2: Typical measured on-resistance.

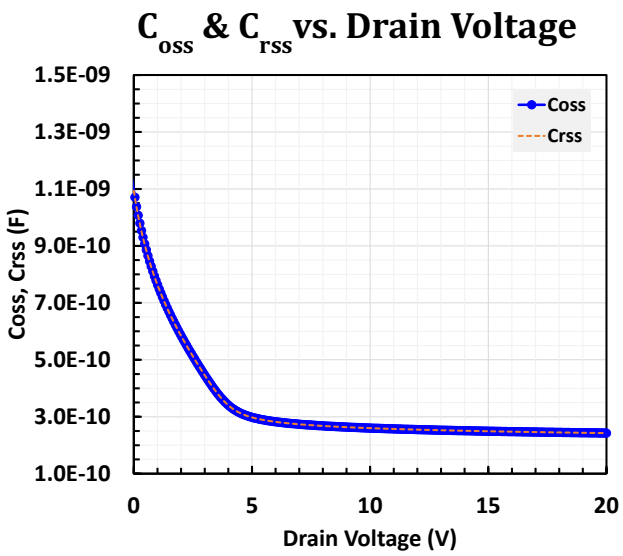


Figure 3: Typical measured output capacitance and reverse capacitance.

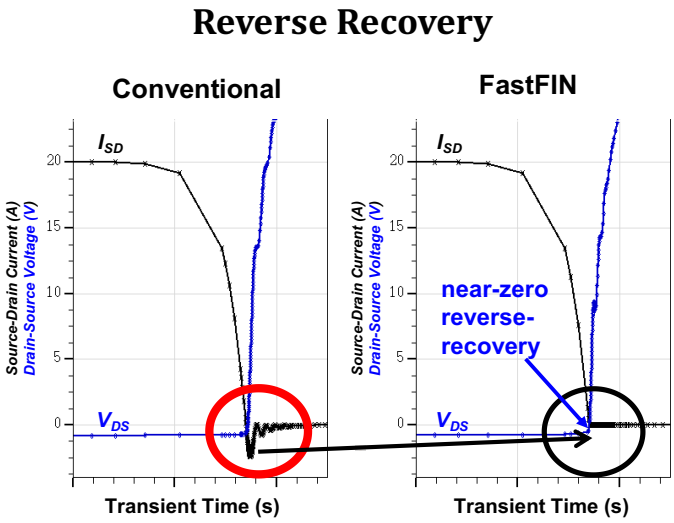


Figure 4: 2D TCAD simulation projected reverse-recovery characteristics.