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DARPA Unveils Research Partners

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7/24/2018 08:30 AM EDT

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Four projects in post-Moore's-law effort detailed

SAN FRANCISCO — Chip giants IBM, Intel, Nvidia, and Qualcomm and a little-known foundry called Skywater were among eight companies announced as prime contractors in four research projects sponsored by the U.S. Defense Advanced Research Projects Agency (DARPA). Many others, including Arm and Globalfoundries, will act as subcontractors in the programs officially launched at an event here today.

The four projects are part of DARPA's Electronics Resurgence Initiative (ERI) expected to receive $1.5 billion over the next five years to drive the U.S. electronics industry forward. They aim to both serve the needs of the U.S. Department of Defense and to boost the semiconductor industry at a time of diminishing returns pursuing Moore's law to make faster, cheaper, smaller chips.

"A 53-year old exponential is unheard of … when it slows or does something different, it's incredibly frightening from a researcher's perspective," said William Chappell, who heads DARPA's microsystems office that oversees ERI. "Our goal is to impact the industry in 2025 to 2030 with research beyond what companies would be looking at today."

Other companies acting as prime contractors for the latest four projects include Applied Materials, Ferric Inc., and HRL Laboratories. In addition, researchers from Mentor Graphics and Xilinx recently joined DARPA to help manage ERI programs.

The industry participation is "a very good start, but it's not all-inclusive, and we want to build on these relationships," said Chappell, noting that DARPA plans to announce another handful of programs this fall.

In one of the largest of the programs, Skywater Technology Foundry aims to show how it can define a monolithic 3D capability to deliver the equivalent of 7-nm chips using its base 90-nm process. The foundry was formed around a former Cypress fab in Minnesota.

Skywater will work with researchers from MIT and Stanford on DARPA's 3DSoC program. It aims to find ways to integrate novel materials such as resistive RAMs and carbon nanotubes on a base low-temperature 90-nm process. Its success will be measured in terms of yields on devices that could slash computing times as much as 50x.

The project is one example of how DARPA aims, in part, to bolster chip-making in the U.S. Separately, DARPA will work with Globalfoundries on MRAM and future memories in a

program called Foundations Required for Novel Compute (FRANC).


Chappell

"The U.S. has more 14-nm fabs than anywhere in the world, but we don't have relationships to tap into them all … our intent is to tap into [fabs at companies such as] Micron, On, TI, Samsung in Austin, and others," said Chappell, noting that DARPA has multiple ways to certify trusted federal suppliers, including foundries such as TSMC.

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Programs explore architecture, design, materials

Among the four new programs, FRANC aims to find new materials and devices to make 10x advances in embedded, non-volatile memories as fast as SRAM but more dense. Prime contractors include Applied Materials, Ferric, HRL, and academics at UCLA and the Universities of Minnesota and Illinois.

Intel, Nvidia, and Qualcomm are prime contractors for the Software-Defined Hardware (SDH) program. They will work with researchers at Georgia Tech, Princeton, Stanford, and the Universities of Michigan and Washington.

SDH aims to define chips that can be reconfigured in real time based on the data being processed. Devices from both SDH and the FRANC program will be measured by the size and speed of graphs that they traverse.

An Nvidia spokesman said that the company's work will span three areas. It will develop domain-specific programming languages targeting tensor algebra, graph analytics, and machine learning. It also will design configurable compute units and memory pipelines and ways to dynamically reconfigure them based on data patterns detected at run time.

One other program, Domain-Specific System on Chip (DSSoC), will include IBM, Oak Ridge National Labs, Arizona State, and Stanford. It aims to find ways to balance applications-specific and general-purpose processing techniques starting with work on software-defined radio. As the project matures, it aims to handle multiple types of accelerators.

The four new programs are part of six programs announced last fall. Details of two of the programs related to EDA were unveiled in late June at DAC.

A networking reception at the ERI Summit attracted researchers and executives. (Image: EE Times)

As part of the programs announced last month, Cadence said that it will work with Carnegie Mellon and Nvidia to define a design flow for chips and boards that can use machine learning. Cadence created a website for its work that includes developing automated methods for routing and tuning of devices to improve reliability and performance.

At the event here, DARPA held brainstorming sessions on AI, photonics, security, and emulation to generate ideas for new programs that it could launch in the fall. More than 450 people attended the half-day workshops, with 180 at the AI session, the largest of the four. Nearly 1,000 researchers attended the overall event.

— Rick Merritt, Silicon Valley Bureau Chief, EE Times

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